Customer No.: 31561
Docket No.: 12681-US-PA
Application No.: 10/708,171

REMARKS

Present Status of the Application

The Office Action rejected claims 1-8. Specifically, claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder (U. S Patent 6,215,135) in view of Chen et al. (U. S. Patent 6,016,002; hereinafter Chen). Claims 1-8 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 103

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder in view of Chen. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The present invention, as for example shown in FIG. 2 and FIG. 3, the two parasitic BJT's are created by specifically forming the two wells 130 and 140 in different conducting type. The source region 110 of the MOS transistor 170 and the drain region 111 of the MOS transistor 180 are connected at the region over the substrate and the two wells 130, 140. As a result, the two doped wells 130 and 140 and the substrate are used to from the BJT 204 while the other BJT 202 is also formed in the substrate using the doped well 130. These two specific BJT's 202 and 204 are created under positive bias using the two wells 130, 140 and the connected source/drain regions 110, 111 over the substrate, the two wells 130, 140. The structures have been clearly recited in independent claim 1 and further in dependent claims 7 and 8.

In re Schroder, Fig. 1 discloses only one well WLL. In equivalent circuit Fig. 2, the BJT T1 is not formed by the two doped well and the substrate, as recited in claim 1. In other words, BJT T1 does not discloses the BJT 204 of the present invention (see FIG. 2).

In addition, the BJT T2 of Schroder is created between the VSS and the VDD. However, the BJT 202 of the present invention is between the source/drain region 110 and 108 but not between the VSS and the VDD.

In other words, Schroder does not disclose the two BJT's in the same way of the present invention.

Furthermore, Schroder does not disclose the two BJT under negative operation (more specifically see in FIG. 3 with respect to claim 8).

Alternatively, Schroder has disclosed the self-completion specific circuit without being modified.

In re Chen, Chen discloses another self-completion circuit as shown in Fig. 3, which has the semiconductor structure in Fig. 4. First, Chen does not intend to modify the circuit in Schroder because the two circuits are self-completion in operation.

In addition, even though Chen discloses two doped wells 98 and 100, Chen does not suggest or provide the motivation to modify the semiconductor structure of Schroder into the semiconductor structure of the claimed invention as recited in claim 1 or further recited in claims 7 and 8.

Only one MOS transistor 78 with the gate 112 in Fig. 4 of Chen is disclosed. There is no

the source/drain region located over the substrate 92, the two doped region 98 and 100 while in comparing with FIG 2 of the present invention. The well region is also used to create the resistor Rp and Rn.

In other words, Chen has its own circuit and does not modify the semiconductor structure of the circuit in Schroder into the present invention. The actual BJT are created under positive bias and the negative bias are further recited in claims 7 and 8.

The present invention has defined the ESD circuit with the semiconductor structure, which is not disclosed either alone or both of Schroder and Chen.

For at least the foregoing reasons, Applicants respectfully submit that independent claim 1 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-8 patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-8 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

Date : June 21, 2005

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